

## Introduction

The Hardware department of Thales Global Services, with a remit traversing all the THALES divisions, has just carried out thermal simulations of a complex electronic component at an unprecedented level of detail. In modelling the FpBGA 208, it has been possible to import all the copper tracks, for the component and the board, in an STL format thanks to the powerful functionality.

## Approaching Reality at the Component

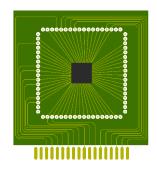
The PCB tracks did not undergo any simplification and the construction of a detailed model proved to be possible in less than one hour of work time. Such a fine-grained representation of reality has never been achieved before.

Thanks to the performance of the solver, the 125-million grid cell model ran during two days on a PC with eight cores with a clock frequency of 3.05GHZ and 48GB of RAM.

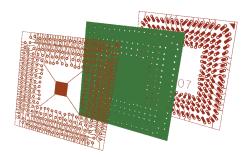
This sets the stage for the next phase in the thermal modelling of electronic components. In view of the technological evolution of packages facilitating "3D design", it has become possible to have increasingly accurate physical representations including precise modelling of complex geometrical shapes, materials with properties that vary with temperature, and parts of very different sizes

Creating a highly detailed model, simulating the thermal behaviour, and validating the results is a vital step in the process of creating an effective compact model—the latter being an RC network (resistor-capacitor) which reproduces, with sufficient precision, the transient thermal behaviour of a real component.

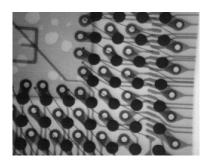
To create a compact model, Thales uses the DELPHI methodology of imposing multiple boundary conditions on a 3D component, and using a genetic algorithm to extract complex RC networks.



Top view of the full 6SigmaET model with the BGA component (drawn in black) mounted on the JEDEC thermal test board



Disassembled view of the 6SigmaET model of a BGA 208 substrates: upper signal layer, dielectric layer, and lower signal

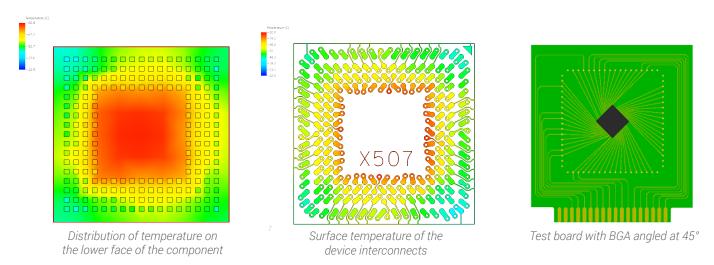


Partial view of the chip and the superposition of its internal electrical cabling

Thales Global Services plays an important role as the creative R&D centre for the Hardware Design teams in Thales group, providing thermal models for the Corporate Component Database that will be used during the design phase of new equipment.

## **Comparison Measurements & Simulations**

The results calculated with 6SigmaET have been compared with measurements carried out by the American company ANALYSIS TECH, in which the component is mounted on a test board corresponding to the JEDEC standard (100mmx110mmx1.6mm). In still air, with the upper face of the board perpendicular to gravity, the thermal resistances Junction / Ambient (RJA) measured for two samples are, respectively, 29.2 °C/W and 30.6 °C/W for a chip power dissipation of 2 W. The value obtained by simulation is 30.1 °C/W, in excellent agreement with the measured values.



## **Next Steps**

With this important step in the modelling of electronic components achieved, it is now possible to:

- Embark with confidence on the process of compact modelling
- Verify the design rules of the package, such as the minimal size of the chipPredict the thermal performance of the component in its product environment
- Identify the thermo-mechanical constraints which can damage the reliability of the package, such as the temperature differences between the BGA balls.

In the future, the thermal performance of the BGA 208 package will be calculated by simulation in other scenarios, including:

- Using a JEDEC board without an internal copper plane (2S0P)
- Cooling of the board by forced convection
- · A transient treatment of the board
- Different orientations of the BGA component

6SigmaET, a computational fluid dynamics (CFD) simulation tool, brings new levels of productivity to electronics cooling design. Thanks to its ease-of-use, it overcomes many of the problems that have plagued analysis tools from the beginning. Boasting substantial automation and intelligence, 6SigmaET is already being used by a global community of design engineers.